facilitates simplifying the manufacturing process, and suppressing the breakdown voltage variations due to induced charges.

[0058] Thus, a superjunction semiconductor device has been described according to the present invention. Many modifications and variations may be made to the techniques and structures described and illustrated herein without departing from the spirit and scope of the invention. Accordingly, it should be understood that the devices and methods described herein are illustrative only and are not limiting upon the scope of the invention.

[0059] This application is based on and claims priority to Japanese Patent Application 2010-250,427, filed on Nov. 9, 2010. The disclosure of the priority application in its entirety, including the drawings, claims, and the specification thereof, is incorporated herein by reference.

What is claimed is:

1. A semiconductor device comprising:

a heavily doped semiconductor substrate of a first conductivity type;

a first alternating-conductivity-type layer comprising a column-shaped or a layer-shaped first semiconductor region of the first conductivity type and a column-shaped or a layer-shaped second semiconductor region of a second conductivity type, the first and second semiconductor regions adjoining each other and repeating in parallel to a surface of the semiconductor substrate in order to form a pn-junction, wherein the pn-junctions extend perpendicularly to the surface of the semiconductor substrate and wherein the first alternating-conductivity-type layer is a drift layer that makes a current flow in an ON-state of the semiconductor device and sustains a voltage in an OFF-state of the semiconductor device;

a surface structure on a surface side of the first alternating-conductivity-type layer, the surface structure constituting an active section that makes the current flow;

an edge-termination section surrounding the active section;

a second alternating-conductivity-type layer in the edge-termination section, the second alternating-conductivity-type layer comprising a column-shaped fourth semiconductor region of the second conductivity type in a third semiconductor region of the first conductivity type, the third and fourth semiconductor regions adjoining each other and repeating in parallel to the surface of the semiconductor substrate to form a pn-junction, wherein the pn-junctions extend perpendicularly to the surface of the semiconductor substrate;

wherein a width of the fourth semiconductor region in the second alternating-conductivity-type layer becomes narrower at a predetermined rate from an edge on a side of the active section toward an edge of the edge termination section.

2. The semiconductor device according to claim **1**, further comprising guard rings in a surface portion of the second alternating-conductivity-type layer, the guard rings being spaced apart from each other.

3. The semiconductor device according to claim **1**, further comprising electrically conductive field plates on the guard rings, the field plates being in electrical contact with the guard rings.

4. The semiconductor device according to claim **1**, wherein the pitch of the alternating first and second type regions in the active section is the same as the pitch in the edge termination section.

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